

12.5 A 25 μ W 100kS/s 12b ADC for Wireless Micro-Sensor Applications

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Micro-sensor nodes are highly energy-constrained and have time-varying performance demands. Accordingly, in this work an ultra-low-power energy-scalable ADC is presented. The SAR architecture is well suited to environment monitoring. Recent micro-power implementations have been limited to low resolutions (8 bits) [1]. The circuit and architecture enhancements presented in this paper efficiently increase precision to 12 bits.

The ADC has two resolution modes: 12b and 8b. In 12b mode, its sampling rate is scalable, at a constant FOM, from 0 to 100kS/s, and, in 8b mode, from 0 to 200kS/s. At the highest performance point (i.e., 12b, 100kS/s) the entire ADC (including all digital, analog, and reference circuitry) consumes 25 μ W from a 1V supply. Several techniques have enabled this low-voltage low-power performance. Analog offset calibration in the latch improves the comparator power-delay product; weak-inversion operation increases the preamp g_m/I ; robust self-timing eases settling requirements; and switched-capacitor auto-zero reference generation maximizes common-mode rejection.

Figure 12.5.1 shows the block diagram of the ADC. In the associated waveforms, the sampling rate is scaled to half the full rate. An input pulse, CNVRT, initiates the conversion. However, as explained later, acquisition is delayed to enhance the noise performance and common-mode rejection of auto-zeroing. Upon completion, the SAR control logic asserts a SLEEP signal to disable the digital state machine and power down the comparator; this enables a larger scaling range than bias-current adjustment [2]. Resolution scaling occurs via two mechanisms. First, bit-cycling is stopped at the desired precision, yielding linear power savings. Additional power savings are achieved in the preamps by selecting between comparator paths (shown in Fig. 12.5.2) optimized for the gain and noise requirements of the precision mode.

Signal levels in the preamp cascade are limited by the low supply voltage. Active bias generation, to store a suitable offset on the coupling capacitors, is avoided. Instead, the preamp common-mode output is designed so that the capacitors can simply be purged and zeroed as shown in Fig. 12.5.2.

The power consumption of the noise-limited preamps increases due to the low supply voltage. Further, previous work shows that, from 8 to 12 bits, the efficiency of comparator-based SAR ADCs degrades as compared to $\Delta\Sigma$ converters. To address this, the gain requirements of the preamps are eased by introducing an offset-compensating regenerative latch. Regenerative amplifiers have a superior power-delay product compared to linear stages [3]. The circuit used is shown in Fig. 12.5.3 (grey devices are deactivated by applying a rail voltage to their gates). M5-6 form regenerative loads, M1-2 are input devices whose sources are selectively decoupled, and M3-4 are biasing current sources. Operation occurs in two phases. However, a calibration reference is required only once, making the structure suitable for multi-step SAR conversion.

The auto-zeroing phase occurs at the start of a conversion and calibrates the differential offset at $V_{SRC1,2}$, the source nodes of M1-2. A zero-differential input, V_Z , is applied, and S_{DIFFMD} is closed, biasing M3-4/M11-12 under the constraint of equal $V_{SRC1,2}$. Then, S_{DIFFMD} and S_{CSCD} are opened. Ignoring the feedback connections through S_{FB} , $V_{HG1,2}$ are high-impedance nodes, where incremental

differences in branch currents are amplified. The resulting voltages are sensed and fed back (through S_{FB}) to rebias M3-4. The branch currents then return to their original values, ensuring equal $V_{SRC1,2}$.

In the reset-resolve phase, S_{DIFFMD} is initially open and the differential input to be resolved appears at the calibrated source nodes. However, the branch currents are set by M3-4 and regeneration is disabled in M5-6 by applying a static bias to their gates. As a result, the voltages generated across $C_{R1,2}$ hold M5-6 in a metastable state. Once regeneration is enabled, closing S_{DIFFMD} perturbs the branch currents depending on the input voltages and the latch resolves. M7-8 are initially configured as low-impedance diode-connected loads. This prevents large differential voltage swings at the drains of M1-2, which, because of finite $r_{o1,2}$, would disturb the $V_{GS1,2}$ calibration.

The support of single-ended inputs, to reduce system complexity, requires special treatment of common-mode signal components. In weak-inversion region of operation, device mismatch and finite r_o limit the CMRR of the comparator. This limitation is mitigated in two ways: (1) common-mode independent acquisition, and (2) preamp auto-zeroing to the voltage of critical SAR decisions. First, the capacitor arrays are purged. During sampling (shown in Fig. 12.5.4), their top-plate floats and only differential-mode charge is sampled. Since half the input is sampled on each array, the DAC outputs always remain within the rails [4]. However, the resulting top-plate voltage may not be suitable for auto-zeroing. Instead, an appropriate reference is generated before acquisition by switching the capacitor arrays as shown in Fig. 12.5.4. Separating the two operations also allows optimization of the auto-zero settling time and noise contribution, minimizing the preamp power-delay product.

Bit-cycling is self-timed so that the DAC and preamps begin settling to their subsequent values immediately after the latch resolves [4]. Since critical decisions never occur successively, overall settling requirements are relaxed, reducing power consumption. To avoid stalling the SAR process, sustained metastability is detected in the latch, and bit-cycling is enforced.

The ADC is fabricated in a 0.18 μ m, 5M2P CMOS process (Fig. 12.5.7). In 12b mode, the measured DNL and INL (Fig. 12.5.5) are +0.58/-0.66LSB and +0.68/-0.56LSB, respectively. The SNDR, with a 48kHz input tone, is 65dB (10.55 ENOB), and the SFDR (Fig. 12.5.6) is 71dB. The total power consumption of the ADC is 25 μ W in 12b mode at 100kS/s and decreases linearly towards zero as the sampling rate is reduced. This corresponds to a FOM of 165fJ/conversion-step. At 500S/s, the power is measured to be 200nW.

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References:

- [1] M. Scott, B. Boser, and K. Pister, "An Ultra Low-Energy ADC for Smart Dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123–1129, July, 2003.
- [2] I. Ahmad and D. Johns, "A 50MS/s (35mW) to 1kS/s (15 μ W) Power Scalable 10b Pipelined ADC with Minimal Bias Current Variation," *ISSCC Dig. Tech. Papers*, pp. 280–281, Feb., 2005.
- [3] J.-T. Wu and B. A. Wooley, "A 100MHz Pipelined CMOS Comparator," *IEEE J. Solid State Circuits*, vol. 23, no. 6, pp. 1379–1385, Dec., 1988.
- [4] G. Promitzer, "12-bit Low-Power Fully Differential Noncalibrating Successive Approximation ADC with 1MS/s," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1138–1143, July, 2001.

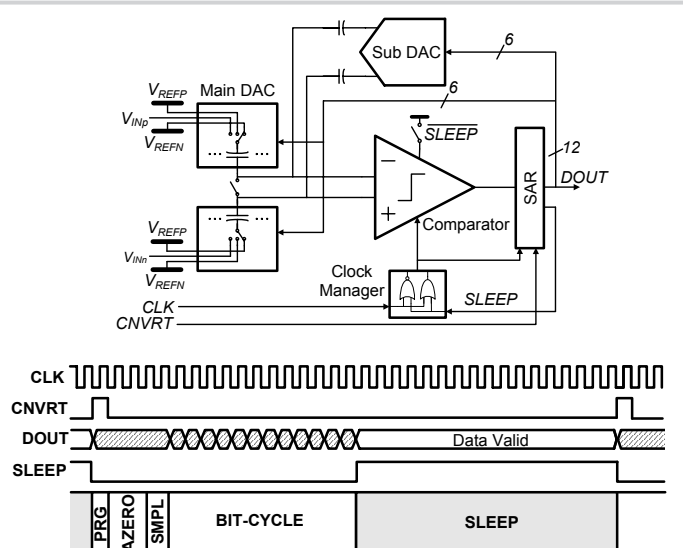


Figure 12.5.1: ADC block diagram and conversion control.

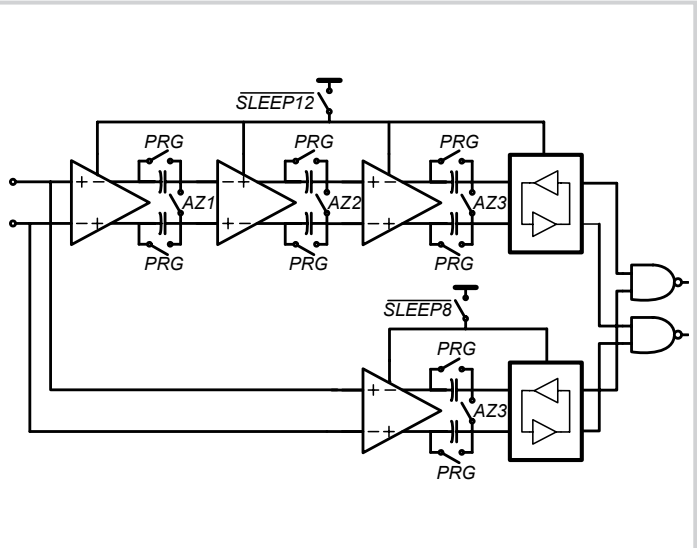


Figure 12.5.2: Comparator block diagram.

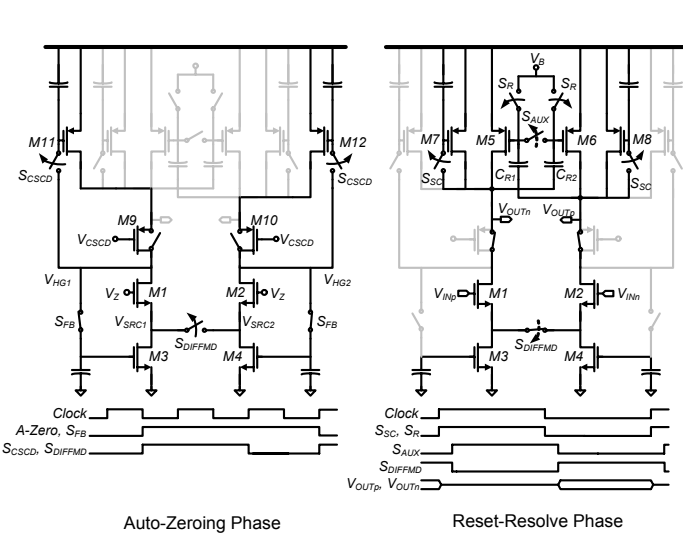


Figure 12.5.3: Offset calibrating regenerative latch.

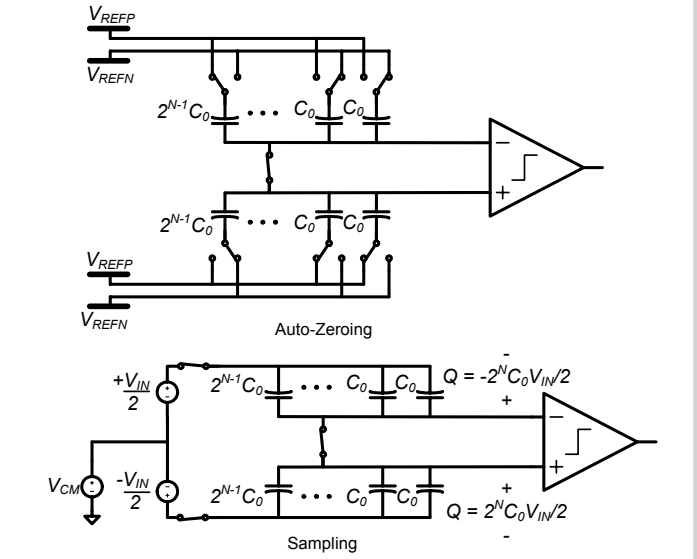


Figure 12.5.4: Auto-zeroing and input sampling networks.

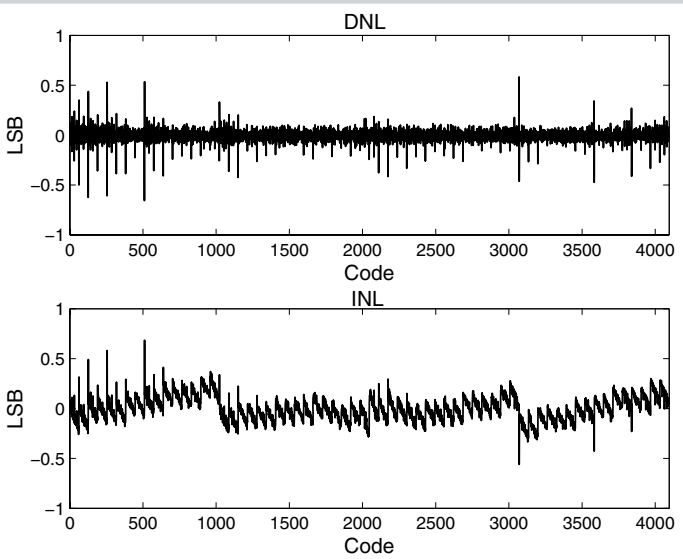


Figure 12.5.5: DNL and INL.

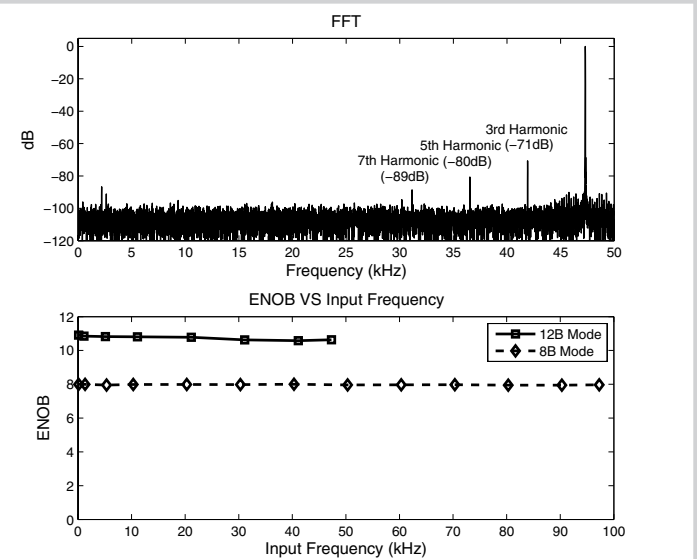


Figure 12.5.6: FFT (for near Nyquist operation) and ENOB plot.

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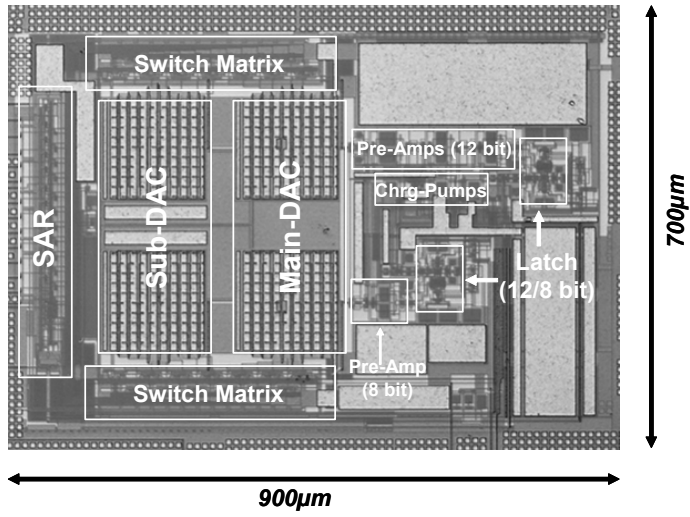


Figure 12.5.7: Die micrograph.