Prediction of Variation in Advanced Process Technology Nodes

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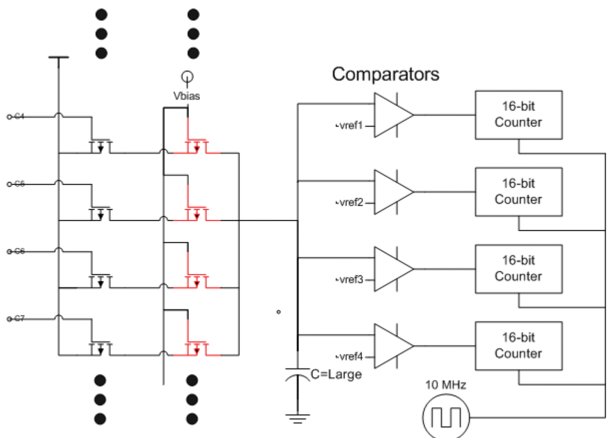
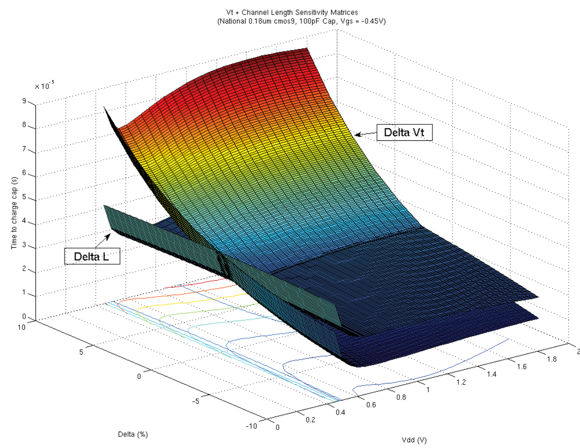
As Moore's Law forces the semiconductor industry into the sub-50-nm regime, process variability is proportionally becoming larger. Design cycles must simultaneously accommodate this increase in process variability and are thus being extended in order to ensure product robustness in the face of such manufacturing uncertainty. To facilitate the designer's need to accurately model and simulate circuits in the face of variation, we seek to provide predictive statistical models for advanced technology nodes and/or novel transistor architectures. Coupled with predictive technology models (PTM) [1], these statistical models will allow designers to simulate designs in a robust manner during, or even prior to, the development phase of a new process technology.

As a basis for providing such models, we are developing simple digital circuits that ease the measurement and extraction of parameters. An example of such a circuit appears in Figure 1. This circuit employs a delay-based measurement to measure the current drive of each of the transistors highlighted in red. If the transistor is biased in the sub-threshold regime and the DIBL coefficient of the process is small enough, we can use the delay measurement as a proxy for threshold-voltage (V_T) variation (i.e., variations in time to charge the capacitor and disable the counter are dominated by V_T variation as Figure 2 shows). However, if the DIBL coefficient is large enough, ΔV_T is no longer as dominant a source of current variation due to the increasing effect of channel-length variation (ΔL). As a result, the circuit no longer functions as a proxy for V_T variation. Nevertheless, the same circuit can be used to determine I_{ON}/I_{OFF} and the sub-threshold slope of a given transistor. In advanced process technologies, a primary factor in determining the viability of the process will be the performance of the process with regard to short-channel effects (SCE), among which the I_{ON}/I_{OFF} ratio and subthreshold slope are extremely significant. Furthermore, the SCE performance of novel transistor architectures such as the FinFET depends heavily on new critical dimensions such as body (fin) thickness [2]. The ability to efficiently measure variability due to such critical dimensions will enable quick determination of process feasibility. Future work includes fabrication of the aforementioned circuit on both mature as well as novel processes such as a FinFET process. Additionally, we would like to identify other circuits capable of such variation measurement to enable us to build complete statistical models.



▲ Figure 1: Circuit to measure sub-threshold variability performance.



▲ Figure 2: Circuit sensitivities to variation in V_T and L vs. V_{DD}.

REFERENCES

[1] Y. Cao, T. Sato, D. Sylvester, M. Orshansky, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," in *Proc. of CICC*, pp. 201-204, 2000.

[2] S. Xiong and J. Bokor, "Sensitivity of double-gate and FinFET devices to process variations," *IEEE Tran. on Electron Devices*, pp. 2255-2261, Nov. 2003.