Near-room-temperature Processed Metal Oxide Field Effect Transistors for Large-area Electronics

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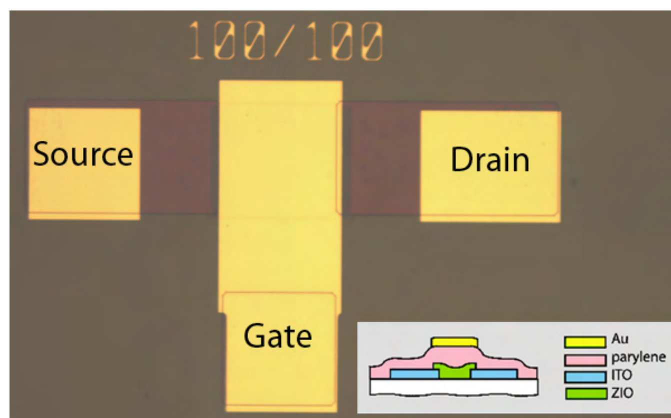
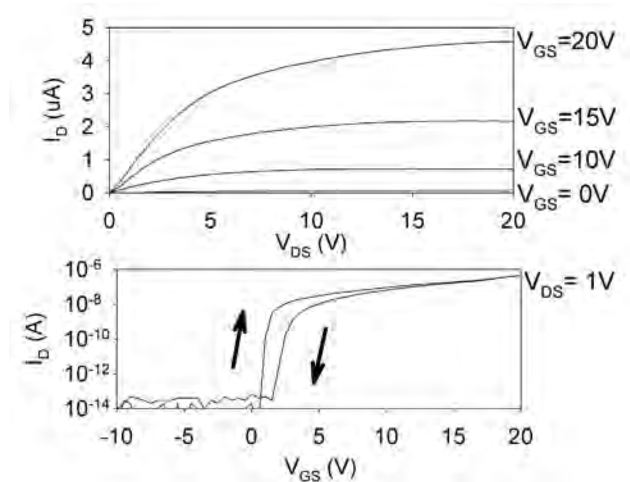
Recently, sputtered metal-oxide-based field effect transistors (FETs) have been demonstrated with higher charge carrier mobilities, higher current densities, and faster response performance than amorphous silicon FETs, which are the dominant technology used in display backplanes [1-2]. Furthermore, the optically transparent semiconducting oxide films can be deposited in a near-room-temperature process, making the materials compatible with future generations of large-area electronics technologies that require use of flexible substrates. [3]. It is possible to process FETs by shadow-mask patterning, but this method limits the range of feature sizes, accuracy of pattern alignment, and scalability of the process to large substrates. Consequently, our project aims to develop a low-temperature, lithographic process for metal oxide-based FETs, similar to one developed for organic FETs [4], that can be integrated into large-area electronic circuits.

Using an organic polymer, parylene, as the gate dielectric and indium-tin-oxide (ITO) for source/drain contacts, top-gate, lithographically processed FETs have been fabricated on glass substrates using $ZnO{:}In_2O_3$ channel layers. Figure 1 shows a micrograph of a completed FET, with current-voltage characteristics shown in Figure 2.

A reproducible FET process requires consistent control of material properties of the metal oxide semiconductor film. We examine the effect of varying deposition conditions (e.g., target composition, O_2 partial pressure, film thickness) and post-deposition treatment on DC- and RF-sputtered amorphous oxide thin films in the In_2O_3-ZnO system. The electrical properties of thin films are determined through resistivity and Hall measurements. These measurements are used as a guide to determine processing conditions for the fabrication of oxide-based field effect transistors and circuits.



▲ Figure 1: Top-view photomicrograph of lithographically patterned field effect transistor (W/L = 100µm/100µm). A schematic cross-section is also shown (inset).



▲ Figure 2: Current-voltage output characteristics (top) and transfer characteristics (bottom) for lithographically patterned zinc-indium-oxide field effect transistor. The transfer curve shown is a double sweep taken in the triode region (W/L = 100µm/100µm).

REFERENCES

[1] R.L. Hoffman, B.J. Norris, and J.F. Wager, "ZnO-based transparent thin-film transistors," *Applied Physics Letters*, vol. 82, no. 5, pp. 733-735, Feb. 2003.

[2] P.F. Carcia, R.S. McLean, M.H. Reilly, and G. Nunes, "Transparent ZnO thin film transistors fabricated by rf magnetron sputtering," *Applied Physics Letters*, vol. 82, no. 7, pp. 1117-1119, Feb. 2003.

[3] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488-492, Nov. 2004.

[4] I. Kymissis, A.I. Akinwande, and V. Bulović, "A lithographic process for integrated organic field-effect transistors," *Journal of Display Technology*, vol 1, no. 2, pp. 289-294, Dec. 2005.