

A Micropower DSP Architecture for Self-powered Microsensor Applications

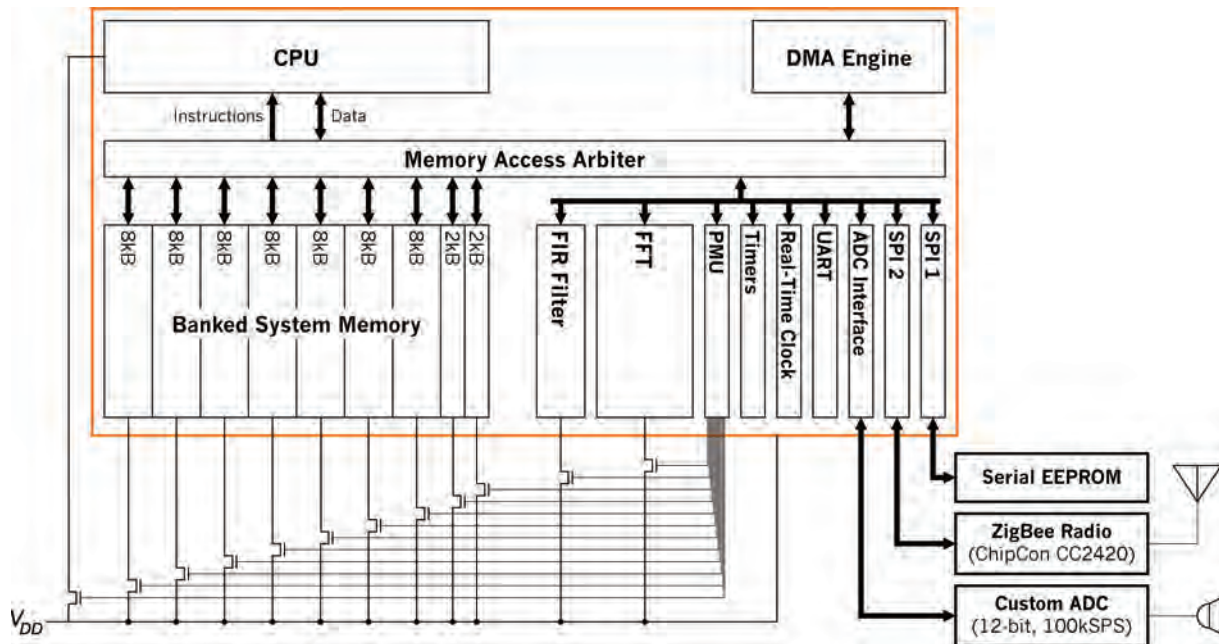
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Distributed microsensor networks consist of hundreds or thousands of miniature sensor nodes. Each node individually monitors the environment and collects data as directed by the user, and the network collaborates as a whole to deliver high-quality observations to a central base station. The large number of nodes in a microsensor network enables high-resolution, multi-dimensional observations and fault-tolerance that are superior to more traditional sensing systems. However, the small size and highly distributed arrangement of the individual sensor nodes make aggressive power management a necessity.

The aim of our project is to develop a micropower DSP platform optimized for medium bandwidth microsensor applications, such as acoustic sensing and tracking. These applications require significant signal processing capability at each node within a sensor network, while maintaining a roughly 100 μ W average power consumption to enable self-powered (energy scavenging) operation. As illustrated in Figure 1, our DSP includes a general-purpose

processor core with an energy efficient instruction set, as well as coprocessors for accelerating Fourier transforms and FIR filtering. Power consumption in the large (62kB) on-chip memory is reduced by dividing the memory into banks (to reduce access energy) and by power-gating inactive banks (to reduce leakage energy). The CPU, FIR, and FFT cores are also power-gated. The DSP was fabricated in 90-nm CMOS by ST Microelectronics.

As part of ongoing work to develop a lightweight, power-aware operating system, the power-gating mechanisms have been characterized with respect to wakeup and energy break-even times. This information is being used to develop scheduling and memory management mechanisms that efficiently utilize power gating. The goal is to automate the details of power management behind standard programming interfaces, exposing only clear and easy-to-use controls.



▲ Figure 1: DSP architecture, illustrating the twelve independent power domains, controlled by off-chip power switches. When combined with an external nonvolatile memory (for program storage), radio, and ADC, the DSP becomes a complete microsensor node.

